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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,212	01/14/2004	Jimmie Earl DeWitt JR.	AUS920030553US1	6480

35525 7590 03/13/2006

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SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,212	DEWITT ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04, 7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/757,212 has a total of 23 claims pending in the application, there are 3 independent claims and 20 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted January 14, 2004 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of both Information Disclosure Statements dated January 14, 2004 and July 1, 2005 are acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

4. Reference BJ on the Information Disclosure Statement dated July 1, 2005 has **not** been considered by Examiner because the reference does not comply with 37 CFR 1.98 (a)(3)(ii). Reference BJ is a non-English-language document, however, there is no copy of an English-language translation of the document, or portion thereof.

OBJECTIONS

Specification

5. The disclosure is objected to because of the following informalities:

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

7. In the section entitled "Cross Reference to Related Applications" Applicant must properly identify all co-pending applications with their corresponding application numbers (i.e. serial numbers).

8. Duplicate copies of pages 81-82 appear in the specification immediately after the first instance of pages 81-82.

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

10. **Claims 9-16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** Claims 9-16 are not limited to tangible embodiments. In view of Applicant's disclosure, pg. 126, line 23 – pg. 127, line 11, the computer readable medium is not limited to tangible embodiments, instead being define as including both tangible embodiments (e.g. recordable-type media, such as a floppy disk, hard disk drive, a RAM, CD-ROMS, and DVD-ROMS) and intangible embodiments (e.g. transmission forms, such as radio frequency and light wave transmissions). As such, claims 9-16 are not limited to statutory subject matter and are therefore non-statutory.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1-2, 4, 8, 9-10, 12, 16-18, 20, and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich et al. (U.S. Patent 6,549,998) in view of IBM Technical Disclosure, "Hardware Cycle Based Memory Residency," hereafter "IBMTD."

13. **As per claim 1**, Pekarich discloses a method in a data processing system for processing instructions, the method comprising:

receiving a threshold value and an identification of one or more addresses to be monitored during the execution of a computer program (col. 4, lines 61-63; col. 3, lines 7-12; col. 1, lines 32-42);

Pekarich does not expressly disclose associating hardware counters with the one or more addresses;

executing the computer program and incrementing respective counters when the one or more addresses are accessed;

and performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

IBMTD discloses associating hardware counters with the one or more addresses (pg. 1, paragraph 3, lines 1-2); It should be noted that each page is associated with a page frame table which is in turn associated with physical addresses.

executing the computer program and incrementing respective counters when the one or more addresses are accessed (pg. 1, paragraph 3, lines 1-2; pg. 1, paragraph 5, line 3);

and performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present (pg. 1, paragraph 5, lines 8-10). It should be noted that "page given immediately to the application requesting it when LRU runs" is analogous to

"performing an action", "the difference between the hardware counter and the PFT counter is greater than the threshold" is analogous to "a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present", and "the difference between the hardware counter and the PFT counter" is analogous to "combination of values obtained from the hardware counters."

Pekarich and IBMTD are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's PFT and hardware counters with Pekarich's address range table.

The motivation for doing so would have been to reduce the expense of operations by allowing more immediate and more cost-effective memory management with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7).

Therefore, it would have been obvious to combine Pekarich and IBMTD for the benefit of obtaining the invention as specified in claim 1.

14. **As per claim 2**, IBMTD discloses arithmetically combining values of the counters to generate a combined counter value (pg. 1, paragraph 5, line 8); It should be noted that "the difference between the hardware counter and the PFT counter" is analogous to "arithmetically combining values of the counters to generate a combined value counter value."

comparing the combined counter value to the threshold value (pg. 1, paragraph 5, lines 8-9);

and performing the action in response to a relationship between the combined counter value and the threshold value being present (pg. 1, paragraph 5, lines 9-10).

15. **As per claim 4**, Pekarich discloses the steps of arithmetically combining values of the counters, comparing the combined counter value, and performing the action are performed in response to incrementing a counter (col. 5, lines 17-23). It should be noted that arithmetically combining values of counters, comparing the combined counter value, and performing the action are all done during separate iterations. The counters must be incremented by either +1 or +2 for the each iteration to occur. Therefore, the counters must first be incremented for the arithmetically combining values of counters, comparing the combined counter value, and performing the action to occur.

16. **As per claim 8**, IBMTD discloses arithmetically combining values of the counters includes combining values in accordance with a condition indicated by a performance monitoring application (pg. 1, paragraph 5, line 8); It should be noted that IBMTD does not specifically disclose a condition indicated by a performance monitoring application, however, it is inherently required that the conditions associated with the process of subtraction be stored somewhere within the system in order for difference calculation between to the "hardware counter" and "PFT counter" to be possible.

17. **As per claim 9**, the claim is rejected for the same reasons as cited in claim 1 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

18. **As per claim 10**, the claim is rejected for the same reasons as cited in claim 2 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

19. **As per claim 12**, the claim is rejected for the same reasons as cited in claim 4 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

20. **As per claim 16**, the claim is rejected for the same reasons as cited in claim 8 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

21. **As per claim 17**, Pekarich discloses an apparatus for processing instructions comprising:

means for receiving a threshold value and an identification of one or more addresses to be monitored during the execution of a computer program (col. 4, lines 61-63; col. 3, lines 7-12; col. 1, lines 32-42); It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

Pekarich does not expressly disclose means for associating hardware counters with the one or more addresses;

means for executing the computer program and incrementing respective counters when the one or more addresses are accessed;

and means for performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present.

IBMTD discloses means for associating hardware counters with the one or more addresses (pg. 1, paragraph 3, lines 1-2); It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

means for executing the computer program and incrementing respective counters when the one or more addresses are accessed (pg. 1, paragraph 3, lines 1-2; pg. 1, paragraph 5, line 3); It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

and means for performing an action in response to a determination that a predefined relationship between the threshold value and a combination of values obtained from the hardware counters is present (pg. 1, paragraph 5, lines 8-10). It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

Pekarich and IBMTD are analogous art because they are from the same field of endeavor, that being memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement IBMTD's PFT and hardware counters with Pekarich's address range table.

The motivation for doing so would have been to reduce the expense of operations by allowing more immediate and more cost-effective memory management with the use of a hardware cycle counter and PFT cycle counter (IBMTD, pg. 1, paragraph 4, lines 5-7).

Therefore, it would have been obvious to combine Pekarich and IBMTD for the benefit of obtaining the invention as specified in claim 1.

22. **As per claim 18**, IBMTD discloses means for arithmetically combining values of the counters to generate a combined counter value (pg. 1, paragraph 5, line 8); It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

means for comparing the combined counter value to the threshold value (pg. 1, paragraph 5, lines 8-9); It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

and means for performing the action in response to a relationship between the combined counter value and the threshold value being present (pg. 1, paragraph 5, lines 9-10). It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

23. **As per claim 20**, Pekarich discloses means for arithmetically combining values of the counters, means for comparing the combined couther value to the threshold value, and means for performing the action operate in response to incrementing a counter (col. 5, lines 17-23). It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

24. **As per claim 23**, IBMTD discloses means for arithmetically combining values of the counters includes combining values in accordance with a condition indicated by a performance monitoring application (pg. 1, paragraph 5, line 8). It should be noted that

pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, see citation note in the rejection for claim 8 above.

25. Claims 3, 6, 11, 14, 19, and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD as applied to claims 1, 9, and 17 above, and in further view of Levine et al. (U.S. Patent 5,797,019).

26. **As per claim 3**, Pekarich/IBMTD disclose a relationship between the combined counter value and the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9).

Pekarich/IBMTD does not expressly disclose generating an interrupt if the predetermined relationship between the combined counter value and the threshold value is present.

Levine discloses generating an interrupt if the predetermined relationship between the counter value and the threshold value is present (col. 11, lines 3-7).

Pekarich/IBMTD and Levine are analogous art because they are from the same field of endeavor, that being processing systems with counters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Levine's threshold invoked interrupt with Pekarich/IBMTD's combined counter value system.

The motivation for doing so would have been to gain the benefit of having the performance monitor facility readily suitable for use in identifying system performance problems through use of appropriate counter values (Levine, col. 11, lines 7-9).

Therefore, it would have been obvious to combine Pekarich/IBMTD and Levine for the benefit of obtaining the invention as specified in claim 3.

27. **As per claim 6**, Levine discloses sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler performs an operation based on receipt of the interrupt (col. 9, lines 30-42; Fig. 4, elements 50, 57, 71, 77, and 79). It should be noted that "performance monitor (PM)" is analogous to "performance monitoring application" and that "interrupt handling routines" are analogous to "operation based on receipt of the interrupt."

28. **As per claim 11**, the claim is rejected for the same reasons as cited in claim 3 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

29. **As per claim 14**, the claim is rejected for the same reasons as cited in claim 6 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

30. **As per claim 19**, Pekarich/IBMTD disclose a relationship between the combined counter value and the threshold value (IBMTD, pg. 1, paragraph 5, lines 8-9).

Pekarich/IBMTD does not expressly disclose generating an interrupt if the predetermined relationship between the combined counter value and the threshold value is present.

Levine discloses generating an interrupt if the predetermined relationship between the counter value and the threshold value is present (col. 11, lines 3-7).

Pekarich/IBMTD and Levine are analogous art because they are from the same field of endeavor, that being processing systems with counters.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Levine's threshold invoked interrupt with Pekarich/IBMTD's combined counter value system.

The motivation for doing so would have been to increase system performance by having the performance monitor facility readily suitable for use in identifying system performance problems through use of appropriate counter values (Levine, col. 11, lines 7-9).

Therefore, it would have been obvious to combine Pekarich/IBMTD and Levine for the benefit of obtaining the invention as specified in claim 19.

31. **As per claim 21**, Levine discloses means for sending the interrupt to an interrupt handler of a performance monitoring application, wherein the interrupt handler performs an operation based on receipt of the interrupt (col. 9, lines 30-42; Fig. 4, elements 50, 57, 71, 77, and 79). It should be noted that pg. 21, lines 4-6 of Applicant's specification appear to define this means as a computer.

32. Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich/IBMTD in view of Levine as applied to claims 3, 11, and 19 above, and in further view of Bartfai et al. (U.S. Patent Application Publication 2003/0101367).

33. **As per claim 7**, Pekarich/IBMTD/Levine disclose all the limitations of claim 7 except the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event.

Bartfai discloses the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event (paragraph 0030, lines 42-45; paragraph 0007, lines 20-22; paragraph 0037, lines 9-14; Fig. 2, element 140). It should be noted that "Fault Service Daemon" is analogous to "log daemon."

Pekarich/IBMTD/Levine and Bartfai are analogous art because they are from the same field of endeavor, that being interrupt handling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bartfai's interrupt logging within Pekarich/IBMTD/Levine's interrupt handling system based on combined counter values.

The motivation for doing so would have been to provide a mechanism for a more complete analysis of adapter error causes (Bartfai, paragraph 00300, lines 46-47).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Levine and Bartfai for the benefit of obtaining the invention as specified in claim 5.

34. **As per claim 15**, the claim is rejected for the same reasons as cited in claim 7 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

35. **As per claim 22**, Pekarich/IBMTD/Levine disclose all the limitations of claim 22 except the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event.

Bartfai discloses the operation is at least one of generating a log entry in a performance monitoring application log and notifying a log daemon process of an event

(paragraph 0030, lines 42-45; paragraph 0007, lines 20-22; paragraph 0037, lines 9-14; Fig. 2, element 140).

Pekarich/IBMTD/Levine and Bartfai are analogous art because they are from the same field of endeavor, that being interrupt handling.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bartfai's interrupt logging within Pekarich/IBMTD/Levine's interrupt handling system based on combined counter values.

The motivation for doing so would have been to provide a mechanism for a more complete analysis of adapter error causes (Bartfai, paragraph 00300, lines 46-47).

Therefore, it would have been obvious to combine Pekarich/IBMTD/Levine and Bartfai for the benefit of obtaining the invention as specified in claim 22.

36. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being obvious over Pekarich in view of IBMTD as applied to claims 1 and 9 above, and in further view of Randall Hyde, "The Art of Assembly Language," hereafter "Hyde."

37. **As per claim 5**, Pekarich/IBMTD disclose arithmetically combining values of the counters (IBMTD, pg. 1, paragraph 5, line 8), comparing the combined counter value (IBMTD, pg. 1, paragraph 5, lines 8-9), and performing the action (IBMTD, pg. 1, paragraph 5, lines 9-10).

Pekarich/IBMTD does not expressly disclose arithmetically combining values of the counters, comparing the combined counter value, and performing the action are performed within microcode of a processor of the data processing system.

Hyde discloses microcode of a processor of a data processing system (pg. 247, section 4.5, 2nd paragraph, lines 2-4).

Pekarich/IBMTD and Hyde are analogous art because they are from the same field of endeavor, that being computer system design.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Hyde's microcode within Pekarich/IBMTD's combined counter value system.

The motivation for doing so would have been to make better reuse of existing silicon on a CPU by using microcode subroutines to implement many common operations (Hyde, pg. 248, section 4.5, 6th paragraph, lines 1-4). Another motivation for doing so would have been to let programmers create some very complex instructions that consist of several different operations, thus providing programmers (especially assembly language programmers) with the ability to do more work with fewer instructions in their programs. In theory, this lets them write faster programs since they now execute half as many instructions, each doing twice the work of a simpler instruction set (Hyde, pg. 248, section 4.5, 7th paragraph, lines 1-4).

Therefore, it would have been obvious to combine Pekarich/IBMTD and Hyde for the benefit of obtaining the invention as specified in claim 5.

38. **As per claim 13**, the claim is rejected for the same reasons as cited in claim 5 above combined with Pekarich's disclosure of a computer program product in a computer readable medium for processing instructions (col. 5, lines 47-65).

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-23** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,113,507 discloses a method and apparatus for a sparse distributed memory system.

2. U.S. Patent 6,681,387 discloses a method and apparatus for instruction execution hot spot detection and monitoring in a data processing unit.

3. U.S. Patent 6,925,424 discloses a method, apparatus, and computer program product for efficient per thread performance information.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
March 1, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER